REMARKS

Claims 1-30, 56-61 and 74-79 are pending in the present application.

In the Office Action, claims 1-30 and 74-79 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. Applicants respectfully traverse the § 112 rejections.

As discussed in the previous response, the specification specifically notes that "trench isolation regions 17 are formed in the active layer 21 to electronically isolate the semiconductor device 10 from other semiconductor devices (not shown)." Specification, page 8, lines 23-24 and Figure 1. As the Examiner well knows, such isolation structures surround the transistor device to electronically isolate the transistor from other devices. Thus, such an isolation structure inherently defines an area. It is respectfully submitted that those skilled in the art would readily understand how isolation structures work based upon the disclosure in the present application and the inherent knowledge of those skilled in the art. For example, the previous response included excerpts from Section 5.4.1.2 of Wolf, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 2 – PROCESS INTEGRATION, 1990 that graphically depict how field isolation regions (not trench isolation structures) are formed to electrically isolate a transistor.

The Examiner nevertheless argues that the specification only provides support for a plurality of trench isolation regions because the specification states that "trench isolation regions 17 are formed in the active layer 21." However, Applicants respectfully submit that the use of the plural term "regions" is a consequence of the cross-sectional depiction of the semiconductor device 10, which results in portions of the trench isolation region 17 appearing on opposite sides of the semiconductor device 10. This does not, however, indicate that the trench isolation region 17 is necessarily formed of multiple elements. To the contrary, persons of ordinary skill in the

art having benefit of the present disclosure should appreciate that the trench isolation region 17 can conventionally be formed as a single entity surrounding the semiconductor device 10 even though it appears as multiple entities in the cross-sectional depiction shown in Figure 1.

Furthermore, Figures 4A-4C of the present application clearly show the back gate electrode 13 extending under the area defined by the isolation trenches 17. It is respectfully submitted that those skilled in the art would read Applicants' disclosure and readily understand that Applicants' disclosure does, in fact, support the claimed subject matter. Applicants respectfully submit that the § 112 rejections should be withdrawn.

In the Office Action, claims 1-30, 56-61 and 74-79 were rejected under 35 U.S.C. § 103 as allegedly being obvious over Inoue (U.S. Patent No. 6,096,582) in view of En (U.S. Patent No. 6,611,023). Applicants respectfully traverse the Examiner's rejections.

A finding of obviousness under 35 U.S.C. § 103 requires a determination of the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed subject matter and the prior art, and whether the differences are such that the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made. *Graham v. John Deere Co.*, 148 USPQ 459 (U.S. S.Ct. 1966). To determine whether the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made, one should determine whether the prior art reference (or references when combined) teach or suggest all the claim limitations. Furthermore, it is necessary for the Examiner to identify the reason why a person of ordinary skill in the art would have combined the prior art references in the manner set forth in the claims. Teaching away by the prior art may constitute *prima facie* evidence that the claimed invention is not obvious.

Independent claims 1, 13 and 23 include, among other things, the limitations that the doped back gate region extends under an entirety of the multiple thickness buried insulation layer and the area defined by the isolation structure. The Examiner has admitted in the Office Action that Inoue does not describe or suggest a doped back gate region that extends under the entirety of the multiple thickness buried insulation layer and the area defined by the isolation structure. The Examiner therefore alleges that En describes a doped back gate region that satisfies the limitations of the pending claims and that it would have been obvious to combine the teachings of Inoue and En to arrive at the subject matter set forth in independent claims 1, 13, and 23. Applicants respectfully disagree. Moreover, Applicants respectfully submit that En teaches away from the Examiner's proposed modification and combination of the cited references.

En describes forming a back gate 38 by performing an implant process through the area occupied by a disposable gate 86. En teaches that the polysilicon gate 34 and the polysilicon back gate 38 must be precisely aligned to avoid degradation of performance due to overlap capacitance caused by gate misalignment. See En, col. 4, ll. 39-51 and Figure 1. Consequently, the back gate 38 in En is a strip that extends along the width of the channel and exactly mirrors the polysilicon gate 34, *i.e.*, the polysilicon back gate 38 extends into the drawing in Figure 3j. See En, col. 6, l. 56 – Col. 7, l. 3. It is also clear from the manner in which the device in En is made that the back gate 38 does not extend laterally, *i.e.*, in the gate length direction, beyond this strip. That is, the back gate 38 in En goes not extend under the source/drain regions 16, 18 shown in En. See En, Figure 3h-3j.

Thus, Applicants respectfully submit that En does not describe or suggest a doped back gate region that extends under an entirety of the multiple thickness buried insulation layer and the area defined by the isolation structure. To the contrary, En teaches away from this claim

limitation. In particular, En teaches that the polysilicon gate 34 and the polysilicon back gate 38 must be precisely aligned to avoid degradation of performance due to overlap capacitance caused by gate misalignment. See En, col. 4, ll. 39-51 and Figure 1. En therefore teaches away from extending the polysilicon back gate 38 beyond the boundaries defined by the polysilicon gate 34 because En teaches that this would lead to degradation of performance due to overlap capacitance caused by gate misalignment. Applicants note that extending the polysilicon back gate 38 in this manner would be required by the Examiner's proposed modification of the prior art.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the subject matter set forth in independent claims 1, 13, and 23 would have been obvious over the prior art of record. Applicants therefore respectfully request that the Examiner's rejections of claims 1-30 and 74-76 under 35 U.S.C. § 103(a) be withdrawn.

Independent claims 56, 58 and 60 recite, among other things, that the doped back gate region as defined in these claims is a doped region that is doped with a dopant material that is of the same dopant type as the dopant material employed in the active layer. For example, if the active layer is doped with a P-type dopant material, *e.g.*, boron, the doped back gate region is also a doped region that is doped with the same type – P-type – dopant material. However, different dopant species – of the same dopant type – may be employed in the active layer and the doped back gate region.

Applicants respectfully submit that independent claims 56, 58 and 60, and all claims depending therefrom, are in condition for allowance. In En, the back gate 38 is doped with a dopant material that is of an opposite type to that of the active layer. En specifically notes that

the channel region 14 is doped with P-type dopant material (Col. 4, ll. 29-32) while the back gate region 38 is formed by implanting an N-type dopant material (Col. 6, ll. 56-61). That is, En teaches exactly the opposite of the subject matter now set forth in amended independent claims 56, 58 and 60. Moreover, there does not appear to be any motivation or suggestion in the art of record that would lead one skilled in the art to modify the express teachings of En so as to arrive at the presently claimed inventions. If anything, En can be thought of as teaching away from the inventions defined in independent claims 56, 58 and 60.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the subject matter set forth in independent claims 56, 58 and 60 would have been obvious over the prior art of record. Applicants therefore respectfully request that the Examiner's rejections of claims 56-61 and 77-79 under 35 U.S.C. § 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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